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(54) Title: METHOD AND APPARATUS FOR DEPOSITING A PLANARIZED DIELECTRIC LAYER ON A SEMICONDUCTOR SUBSTRATE

(57) Abstract

This invention relates to methods and apparatus for treating a semiconductor substrate. The method principally includes treating the substrate by forming on the substrate a liquid short-chain polymer of the general formula R_a Si $(OH)_b$ or R_a SiH_b $(OH)_c$ where a + b = 4 ou a + b + c = 4 respectively; a, b and c are integers, Ri is a carbon-containing group and Si-C bonding is inferred.

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METHOD AND APPARATUS FOR DEPOSITING A PLANARIZED DIELECTRIC LAYER ON A SEMICONDUCTOR SUBSTRATE

This invention relates to methods and apparatus for treating a semiconductor substrate, such as a semi-conductor wafer, and, in particular, but not exclusively, to methods and apparatus for providing a low dielectric constant (known as low k) layer in a planarisation or gap filling operation.

In our earlier co-pending Patent Application WO94/01885, the contents of which are incorporated herein by reference, we describe a planarisation technique in which a liquid short-chain polymer is formed on a semiconductor wafer by reacting silane (SiH_4) with hydrogen peroxide (H_2O_2). The polymer, which initially is in a liquid state, is formed on to a wafer to produce planarisation either locally or globally, or gap filling. This technique provides a planarisation or gap filling layer of silicon dioxide and we have found it to be a most suitable material for semiconductor circuit manufacturing.

However, with the ever increasing demands to enhance device speed and reduce size, there can be problems in more advanced devices with using silicon dioxide as the dielectric insulator between metal lines. The RC time constant associated with the metal lines (or interconnects) on an integrated circuit structure limits the device speed and is a function of the resistance of the interconnections, the thickness of the insulator and its dielectric constant.

Thus in order to reduce the RC time constant and enhance device speed, the options are to modify the characteristics of the interconnect, or the insulator. There are many device design constraints, and practicalities which restrict the designer's freedom and thus we believe it is extremely important to reduce the dielectric constant of the insulator, whilst trying to retain the other desirable properties which make silicon dioxide a suitable material.

For advanced semicoductor devices, dielectric constant values of <3.5 are required and ideally are <3.0. We have found that it is possible to provide a dielectric layer which substantially retains the desirable properties of silicon dioxide but which has a significantly reduced dielectric constant, thereby making it suitable for use in advanced logic devices.

We have also found that the dielectric constant can be reduced by applying a particular set of process conditions.

Accordingly, in one aspect of this invention, there is provided a method of treating a semiconductor substrate, comprising forming on the substrate a liquid short-chain polymer of the general formula $R_aSi(OH)_b$ or $R_aSiH_b(OH)_c$

where a + b = 4 or a + b + c = 4 respectively; a, b and c are integers, R is a carbon-containing group and Si-C bonding is inferred.

The reference to the polymer being 'liquid' is simply intended to indicate that it is neither gaseous not solidified at the moment of formation.

Preferably R is a methyl, ethyl, phenyl or vinyl group,

with methyl (CH_3-) being particularly preferred.

The further polymerisation may be enhanced by heating. It is thought that the liquid short chain polymer undergoes further polymerisation reactions to form an amorphous structure of the general formula

$-(R_x\ Si\ O_y)_n-$ where $x + y = 4$

x and y are integers

R is a carbon-containing group

$n = 1$ to ∞

Si-C bonding is inferred

In another aspect of this invention there is provided a method of treating a semiconductor substrate, which comprises positioning the substrate in a chamber;

introducing into the chamber in the gaseous or vapour state an organosilane containing compound with the general formula C_xH_y-Si_nH_a, and a further compound, containing peroxide bonding, and

reacting the organosilane compound with said further compound to provide on said substrate a short-chain polymer.

According to this invention a liquid short-chain polymer layer is formed on the substrate, the polymer being carbon doped to reduce the dielectric constant of the formed layer. The layer is formed by reacting a silicon containing compound with a compound containing peroxide bonding, and the dopant material may be bound to or otherwise associated with one of the reactants, preferably to the silicon containing gas.

The term peroxide bonding includes hydroperoxide bonds such as O-OH.

Preferably said silicon-containing compound is of the general formula $R\text{-}SiH_3$; R may be a methyl, ethyl, phenyl or vinyl group with methyl (CH_3-) being particularly preferred. Si-C bonding is inferred. Preferably said silicon-containing compound and said further compound may react in a surface reaction on the surface of the substrate. Further polymerisation of the polymer may take place to form an amorphous structure of the general Formula

$$-(R_xSiO_y)_n$$

with the constraints set out above. Further polymerisation may be enhanced by radiative or chemical treatment e.g. by heating.

Preferably the dielectric constant, measured at 1MHz, of said deposited material is less than 3.5 and more preferably less than 3.

The deposition rates may be enhanced by use of a weakly ionized plasma within the process chamber. However, this is at the expense of Si-C bonding and thus the resultant dielectric constant of the deposited layer may be higher than if a plasma had not been used, but it will still be usefully lower than an un-doped silicon dioxide layer. Thus, with some silicon-containing precursors, the use of a plasma enhances the deposition rate without significant detriment to the planarity of the deposited polymer.

The method may further comprise forming or depositing

an under layer or base layer prior to the deposition of the polymer layer. The base layer is preferably deposited using a Chemical Vapour Deposition (CVD) or Plasma Enhanced Chemical Vapour Deposition process (PECVD) before the depositing of the polymer layer. The PECVD or CVD process is preferably carried out in a separate chamber to that in which the polymer layer is deposited, but can be carried out in the same chamber. The under layer may be a doped or un-doped silicon dioxide or other silicon containing layer.

The method may further comprise depositing or forming a capping layer on the surface of the formed layer. This layer is preferably applied in a PECVD process.

Preferably said PECVD or CVD capping process is applied in a chamber separate to that in which the polymer layer is formed. The capping layer may be a doped or un-doped silicon dioxide or other silicon containing layer.

Preferably the PECVD or CVD chamber comprises a platen for supporting the substrate which is maintained at a temperature in the range of from 100°C - 450°C, and more preferably around 350°C.

The method may further comprise chemical or radiative treatment (e.g. heating) of the polymer layer and this heating preferably takes place after capping, as the cap provides mechanical stability for the polymer layer during cross-linking. The polymer layer may be heated to 350°C - 470°C for 10 to 60 minutes. For example the heating may last 30 minutes at 400°C. The heating may be achieved using a furnace, heat lamps, a hot plate, or plasma heating. The

heat treatment step removes excess water from the layer, which is a by-product of the cross-linking reaction. It may also remove SiOH bonds.

In another aspect, this invention provides apparatus for implementing the method as described above which comprises a CVD chamber and PECVD chamber, said CVD chamber having means for introducing therein two or more reaction gases or vapours, platen means for supporting a semiconductor substrate, and means for maintaining the temperature of the platen at a required level, said PECVD or CVD chamber including platen means for supporting a semiconductor substrate, means for introducing one or more reaction gases or vapours, together with means for generating a plasma if required, to cause the gaseous vapours to react.

The invention may be performed in various ways and a specific embodiment will now be described, by way of example, with reference to the following drawings, in which:

Figure 1 is a schematic view of apparatus for performing the treatment method;

Figure 2 is a FTIR analysis of an example of a polymer layer of this invention;

Figure 3 is a graph showing variation of refractive index with heating temperature for a polymer layer in accordance with this invention and two comparative layers;

Figure 4 is a Scanning Electron Micrograph showing the flow property of the polymer layer of this invention, and

Figure 5 is a graph of integrated Si-C and C-H peak

areas versus heating temperature for a polymer layer an embodiment of this invention;

Figure 6 is a graph of dielectric constant versus Si-C/Si-O peak area ratio for the polymer layer in accordance with this invention; and

Figure 7 is a diagram of a chemical structure referred to below.

Apparatus for treating semiconductor substrates , such as semi-conductor wafers is schematically illustrated at 10 in Figure 1. It will be understood that only the features which are particularly required for the understanding of the invention are described and illustrated. The general construction of such apparatus is well known in the art.

Thus, the apparatus 10 includes a chemical vapour deposition (CVD) chamber 11 having a duplex shower head 12 and a substrate support 13. The shower head 12 is connected to RF source 14 to form one electrode, whilst the support 13 may be earthed and may form another electrode. (The RF source 14 is provided to allow etch back of the chamber and chamber furniture for cleaning purposes and/or to provide a weakly ionised plasma during deposition). The shower head 12 is connected by respective pipes 15 and 16 to a source of CH_3SiH_3 in N_2 or other inert carrier and a source of H_2O_2. The carrier gas is conveniently used for ease of operation of the equipment; it is believed that the process could be performed without it.

The source of H_2O_2 comprises a reservoir 17, an outlet pipe 18, a pump 19 and a flash heater 20 for vaporising the

H_2O_2.

In use the CVD chamber may be operated to form a short chain, inorganic polymer, which is initially a liquid, on the surface of a semi-conductor wafer to produce planarisation either locally or globally, or for 'gap filling'. The polymer is formed by introducing into the chamber the methyl silane and the hydrogen peroxide in vapour form and reacting them either in a gaseous reaction or at the wafer surface spontaneously. Once the resultant polymer is formed on the wafer, it has been found that the rate of polymerisation is such that the condensate remains a liquid long enough to allow the polymer to flow. As a consequence the layer fills both small and large geometries or gaps. As the film grows thicker, surface tension tends to cause the film to self planerise. It is believed that effectively this process takes place as the polymerisation takes place. The more settlement which occurs prior to full polymerisation the less likelihood there is of cracking. Very small dimensioned gaps can be filled and because of the fill layer properties these gaps can even, in certain circumstances, be re-entrant.

It has further been found that providing a weakly ionized plasma in the chamber enhances deposition rates, without being significantly detrimental to the properties of the layer. Thus, with some silicon containing precursors, the use of a plasma enhances the deposition rate without significant detriment to the planarity of the deposited polymer.

The apparatus 10 also includes a Plasma Enhanced Chemical Vapour Deposition (PECVD) chamber 24 of generally conventional construction, comprising a shower head 25 and a wafer support 26. The shower head 25 is connected to RF source 27 to form one electrode, whilst the support 26 is earthed either directly on through a variable resistance and forms another electrode. Alternatively the shower head 25 may be earthed and the support may be driven. The shower head 25 is connected by respective pipes 28 and 29 to a source of silane (SiH_4) in N_2 or other inert carrier and a source of N_2O.

In use, the PECVD chamber may be operated to deposit a base layer or under layer on a semiconductor wafer or other semiconductor substrate prior to deposition of the doped polymer layer discussed above. Likewise, after deposition of the polymer layer in the CVD chamber 11, the semiconductor wafer may be returned to the PECVD chamber for plasma deposition of a capping layer. Both the under layer or base layer and the capping layer have a similar chemistry of silicon dioxide.

EXAMPLE

A wafer is loaded into the machine and transferred to the PECVD chamber. A 1000Å base layer of silicon dioxide is deposited at a temperature of 350°C. (The base layer could be between 100Å and 3000Å thick). Whilst still in the PECVD chamber, the wafer may be subjected to pre-treatment with a plasma, for example using a gas such as N_2O, O_2 or N_2.

The wafer is then transferred to the CVD chamber 11

where the polymer layer is formed at a platen temperature of 0°C, to a thickness of 8000Å. The pressure in the CVD chamber 11 during formation of the polymer layer is typically around 850mT. For good quality films and to reduce the dielectric constant, it is desirable to remove as much water and OH from the film at an early stage. The layer is therefore exposed to a reduced pressure (typical 1-2mT) for a period of thirty seconds.

The wafer is then transferred to the PECVD chamber and a capping layer of 1000Å - 6000Å is deposited at a temperature of 350°C. The wafer is then unloaded from the machine and furnace heat treated at a temperature of 400°C for thirty minutes to remove the residual moisture and OH from the film, the inclusion of which would cause the dielectric constant to be higher.

Where the PECVD and CVD process are to be carried out in the same chamber, a wafer loading device 21 can be used to lift the wafer to an intermediate position 23 during heating of the wafer, to avoid unnecessary heating of the support 13.

EXPERIMENT

Analysis of the basic chemistry involved suggested that the Si-H bonds in the SiH_3 component of CH_3-SiH_3 would react with H_2O_2 in a similar manner to the Si-H bonds in SiH_4, leaving the Si-CH_3 bond intact. The resultant film was therefore expected to contain a basic SiO_2 structure with a CH_3 group attached to each silicon atom. An example of such

a structure is shown in Fig 7.

Initial observations confirmed that the doped polymer layer was indeed formed using the new process. The resultant film was then evaluated to confirm that $Si-CH_3$ was present in the film.

In order to confirm that $Si-CH_3$ and C-H bonds were present in the layer, we subjected the layer to Fourier Transform Infra-red (FTIR) analysis and the results are shown in Figure 2, which indicate that both the C-H and Si-C bonds are present.

It is known that the refractive index of a material is related to the dielectric constant. Refractive index measurements confirmed a lower refractive index was obtained for the doped polymer layer following thirty minute furnace heat treating in nitrogen ambient. As discussed above, the heat treating removes residual moisture from the layer. In Figure 3 the results are plotted, for increasing heating temperature, for a polymer layer of this invention "DOPED", for a silane/hydrogen peroxide layer as described in WO94/01885 "ET2" and a hybrid of these two layers "50%/50%". A marked decrease in refractive index was observed for the doped polymer layer in comparison with the layer according to WO94/01885. The hybrid (50%/50%) layer showed a smaller reduction in refractive index which was consistent given the smaller proportion of methyl silane in the source gas.

Scanning Electron Microscope (SEM) observation confirmed that the polymer layer exhibited good flow

properties, as seen in the SEM views given in Figure 4.

Dielectric constant measurements were taken over an average of five wafers produced in accordance with the above example, with 25 capacitors per wafer. The wafers were furnace heat treated prior to measurement at a temperature of 400°C in nitrogen for thirty minutes. The doped polymer layer averaged a dielectric constant of 3.24 at 1MHz.

An important property of any doped oxide layer is its temperature stability. Theory suggests that the Si-C bond should be generally stable to temperatures up to about 400°C, and we had predicted that the same would be true for Si-C bonds within the doped polymer layer. To confirm the temperature stability of the doped polymer layer, a wafer was furnace heat treated in nitrogen ambient at sequentially higher temperatures whilst monitoring both the Si-C and C-H peaks using FTIR. Figure 5 shows a plot of the integrated Si-C and C-H peak areas versus heating temperature. The curves indicate that the Si-C and C-H bonds are stable within the hardened doped polymer layer up to temperatures of at least 400°C after which the areas of the peaks and hence the number of bonds are seen to reduce.

A pump 22 is provided for reducing chamber pressure.

As has been indicated above the methyl silane may be substituted by ethyl, phenyl, vinyl silane or other organic silane and sources of peroxide bonding other than hydrogen peroxide may be used. Further precusors could be employed that provide an Si-C bond that was maintained from the gaseous phase adjacent to the wafer to the resultant

hardened polymeric layer upon the semiconductor substrate.

CLAIMS

1. A method of treating a semiconductor substrate comprising depositing on the substrate a liquid short-chain polymer of the general formula R_a $Si(OH)_b$ or $(R)_aSiH_b(OH)_c$, where a + b = 4 or a + b + c = 4 respectively; a, b and c are integers, R is a carbon-containing group and a silicon to carbon bond is inferred.

2. A method according to Claim 1, wherein R comprises a methyl, ethyl, phenyl or vinyl group.

3. A method of treating a semiconductor substrate, which comprises positioning the substrate into a chamber, introducing into the chamber in the gaseous or vapour state an organosilane compound of the general formula C_xH_y-Si_nH_a, and a further compound containing peroxide bonding and reacting the silicon-containing compound with said further compound to provide on said substrate a short-chain polymer.

4. A method according to Claim 3, wherein said silicon-containing compound is of the general formula R-SiH_3.

5. A method as claimed in Claim 4 wherein R is a methyl, ethyl, phenyl or vinyl group.

6. A method according to Claims 4 or 5, wherein said silicon-containing compound is methyl silane (CH_3SiH_3).

7. A method according to any preceding Claims, wherein said short-chain polymer is formed as a surface reaction.

8. A method as claimed in any one of the preceding claims wherein further polymerisation takes place to form an amorphous structure of the general Formula - $(R_xSiO_y)_n$

9. A method according to any of the preceding Claims, wherein the dielectric constant of said deposited material is measured at 1MHz is less than 3.5.

10. A method as claimed in any one of the preceding claims wherein the deposition rate is enhanced by using a weakly ionised plasma.

11. A method as claimed in any one of the preceding claims further comprising forming or depositing an under layer or a base layer.

12. A method as claimed in any one of the preceding claims further comprising depositing or forming a capping layer on the surface of the formed layer.

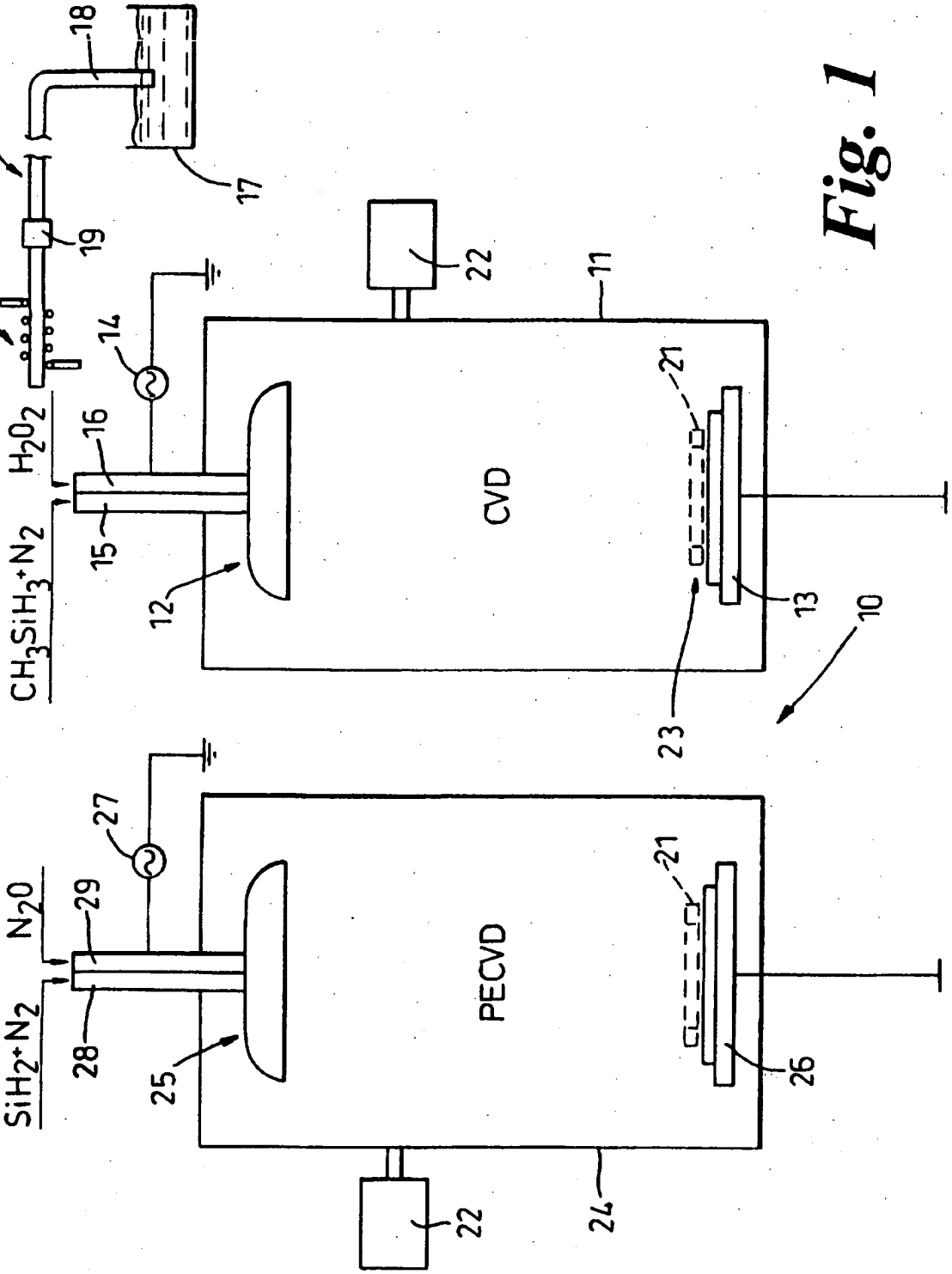
13. A method as claimed in any one of the preceding claims further comprising chemical or radiative treatment of the polymer layer to provide mechanical stability of the layer.

14. Apparatus for implementing the method of any one of the preceding claims comprising a CVD chamber and a PECVD chamber, said CVD chamber having means for introducing therein two or more reaction gases or vapours, platen means for supporting a semiconductor substrate, and means for maintaining the temperature of the platen at a required level, said PECVD or CVD chamber including platen means for supporting a semiconductor substrate, means for introducing one or more reaction gases or vapours, together with means for generating a plasma if required, to cause the gaseous vapours to react.

15. Apparatus as claimed in claim 15 having a single

dual CVD and PECVD function chamber.

16. Apparatus as claimed in claim 16 including means for lifting the substrate from the support for enabling heating of the substrate during PECVD processing without substantial commensurate heating of the support.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19
20
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14
21
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15
12
13
10
23
27
21
N_2O
29
PECVD
SiH_2+N_2
28
25
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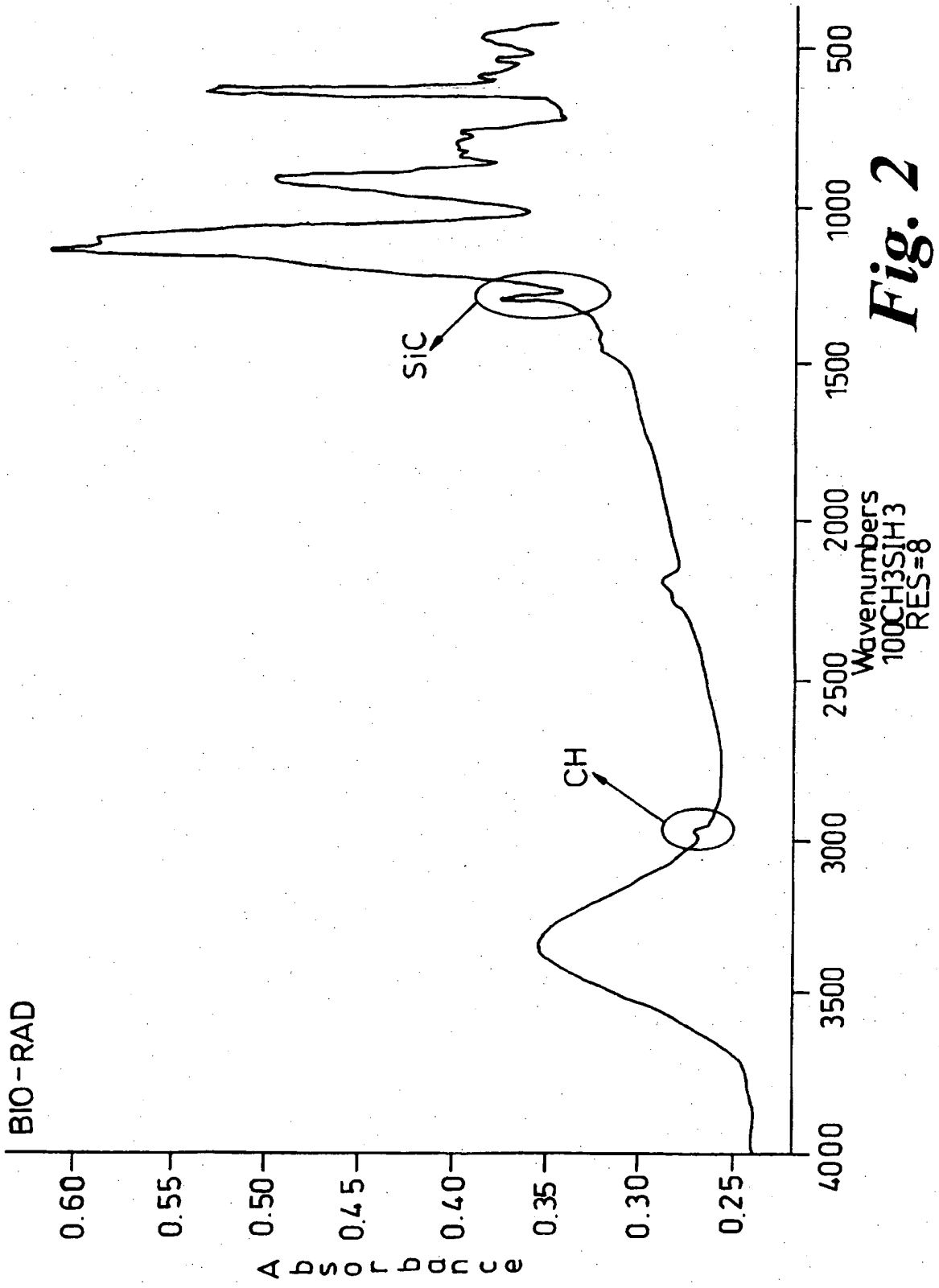
22
24

Fig. 1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RES=8
CH
SiC

Fig. 2

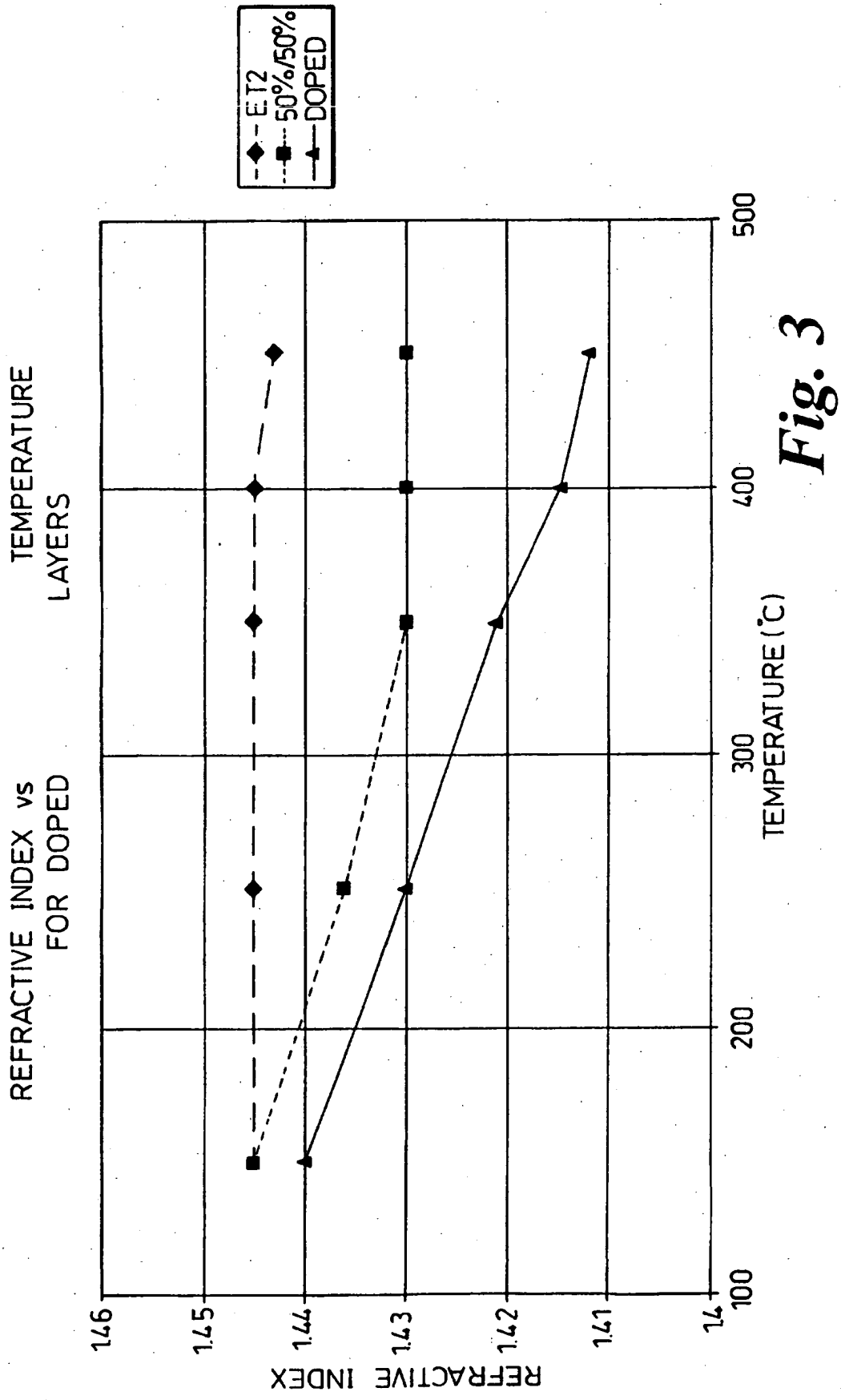

ET2
50%/50%
DOPED
REFRACTIVE INDEX vs TEMPERATURE
FOR DOPED LAYERS
REFRACTIVE INDEX
1.46
1.45
1.44
1.43
1.42
1.41
1.4
100
200
300
400
500
TEMPERATURE (°C)

Fig. 3

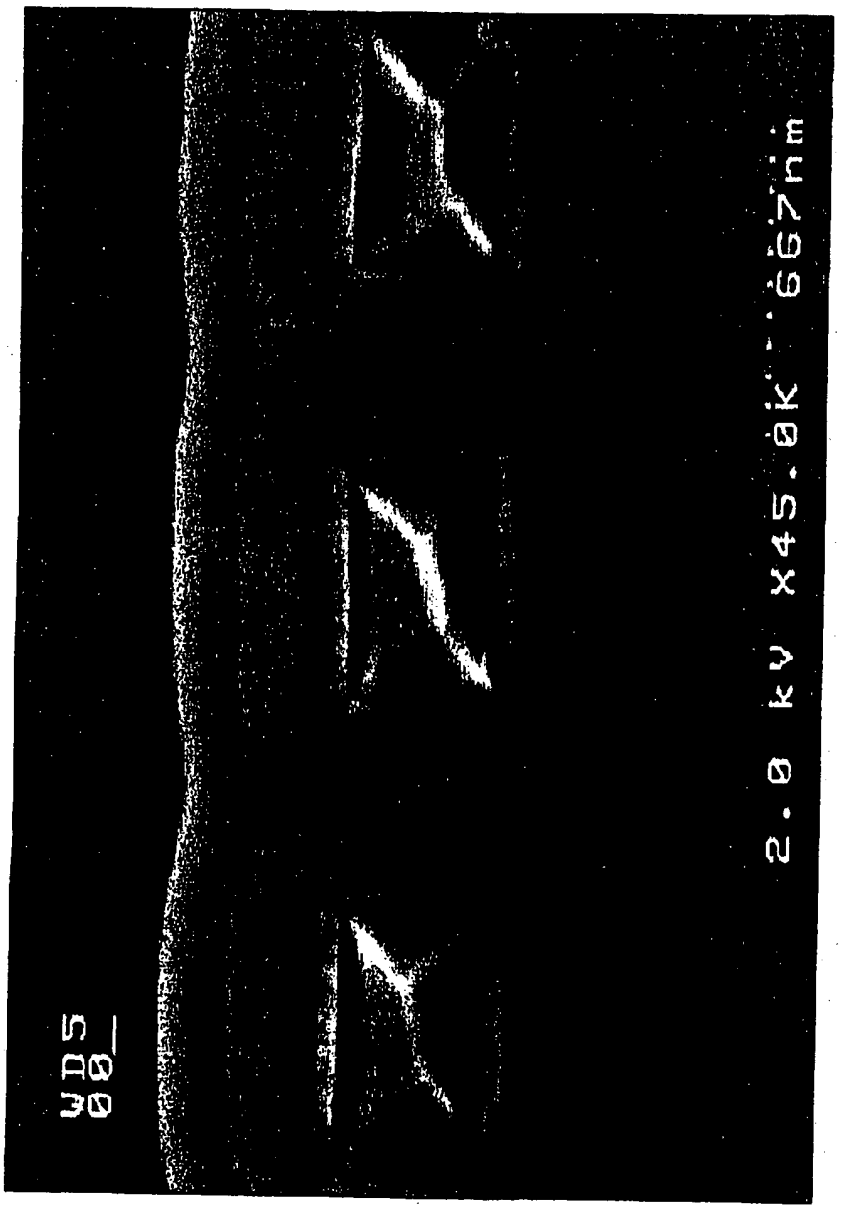


Fig. 4

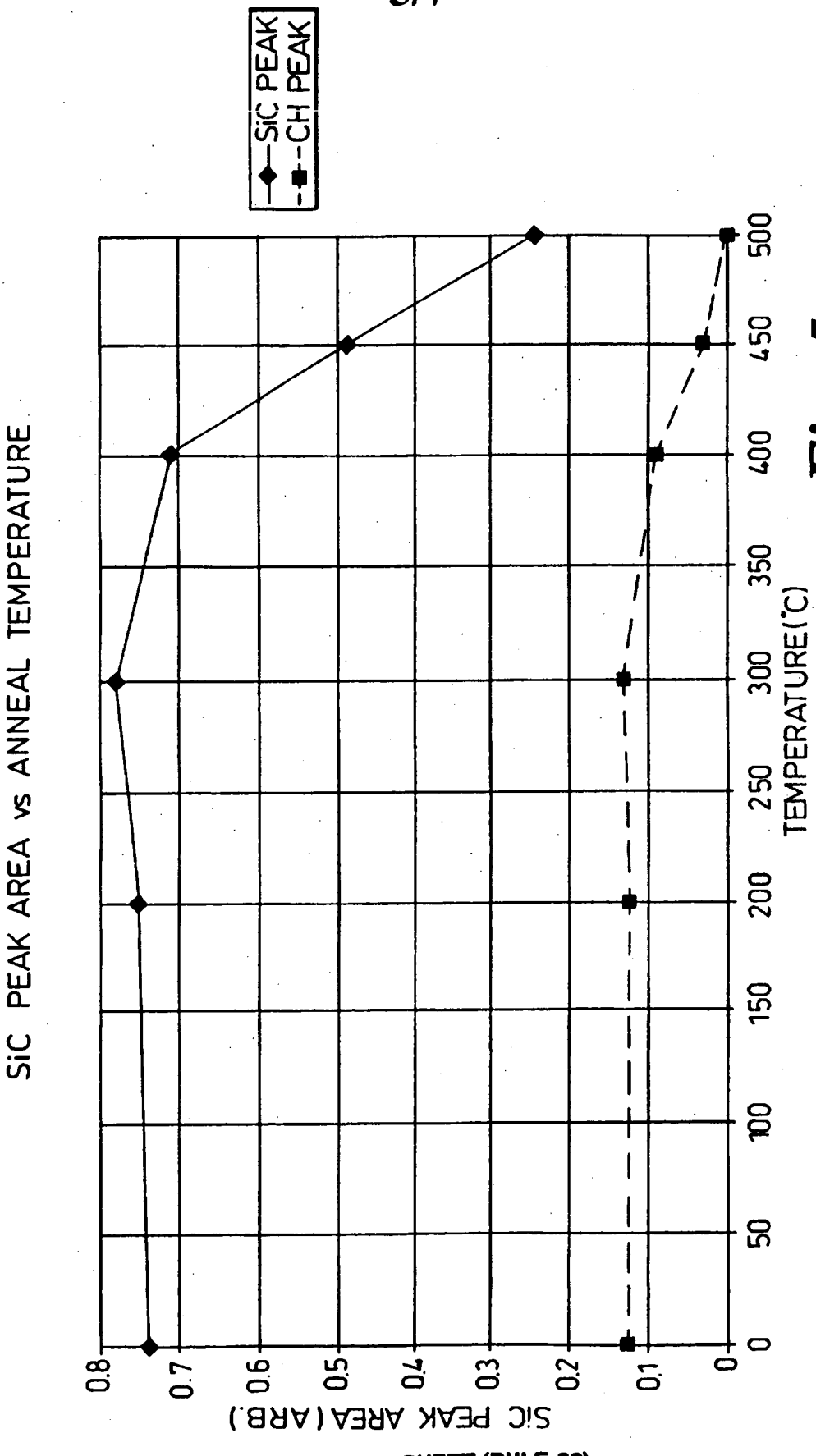
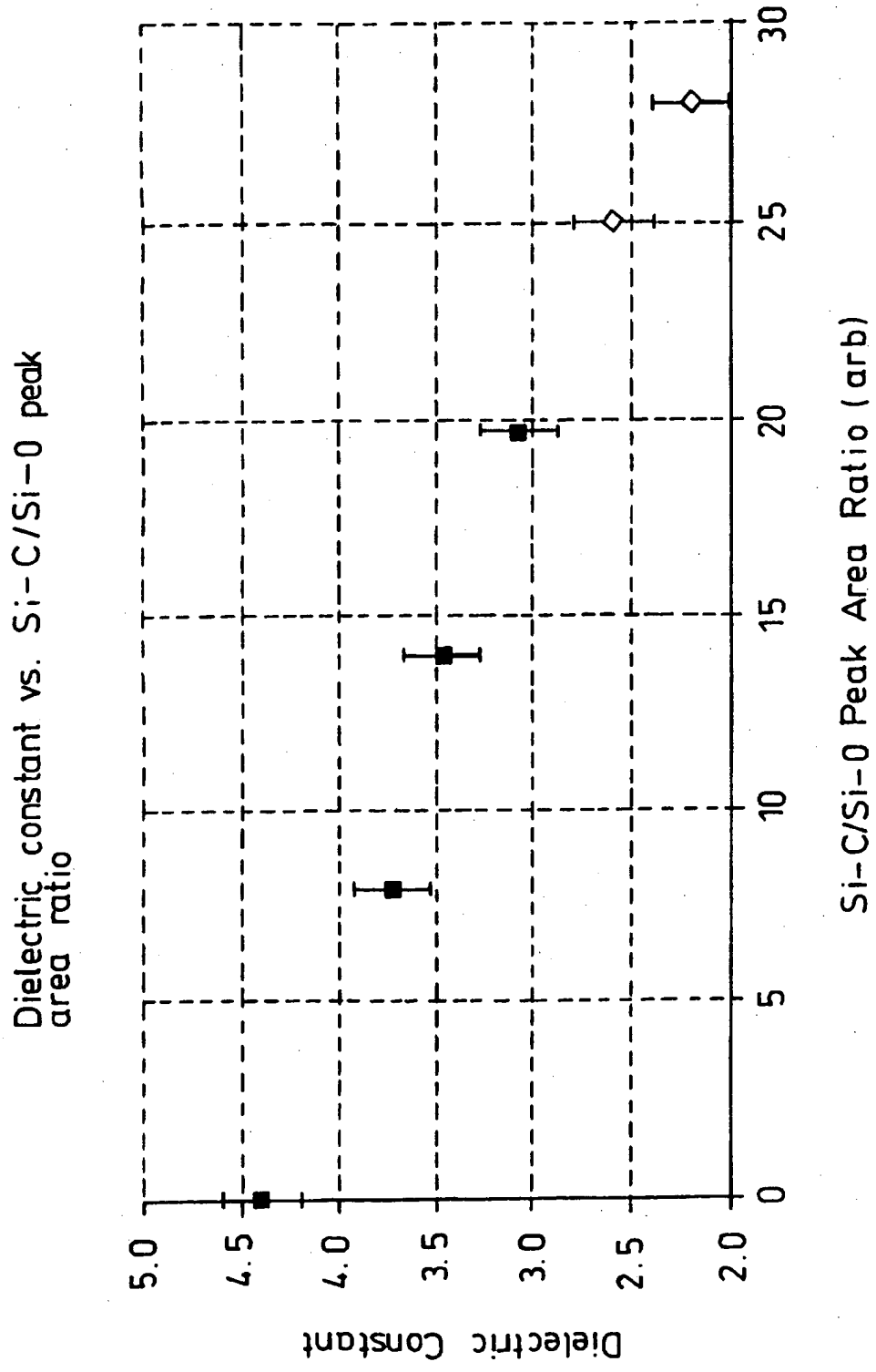

SiC PEAK AREA vs ANNEAL TEMPERATURE
SiC PEAK
CH PEAK
SiC PEAK AREA (ARB.)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
TEMPERATURE(°C)
0
50
100
150
200
250
300
350
400
450
500

Fig. 5


Dielectric constant vs. Si-C/Si-O peak area ratio
Dielectric Constant
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4.5
4.0
3.5
3.0
2.5
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5
10
15
20
25
30
Si-C/Si-O Peak Area Ratio (arb)

Fig. 6

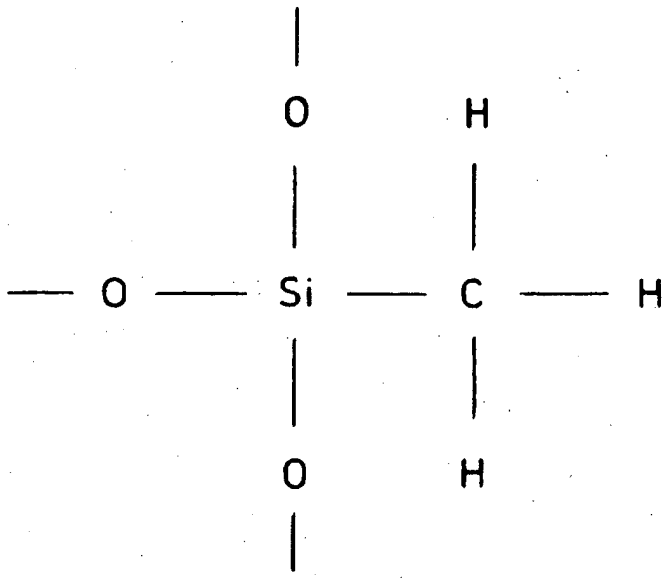

Fig. 7

INTERNATIONAL SEARCH REPORT

Inter.. ..onal Application No
PCT/GB 97/02240

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/312 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 726 599 A (TOKYO SHIBAURA ELECTRIC CO) 14 August 1996 see page 3, line 56 - page 5, line 32	1-5,7-9, 12
A	---	14,15
A	WO 94 01885 A (DOBSON CHRISTOPHER DAVID) 20 January 1994 see page 5, line 56 - page 8, line 32	1-5,7-9, 11,12, 14,15
X	--- M.MATSUURA ET AL.: "NOVEL SELF-PLANARIZING CVD OXIDE FOR INTERLAYER DIELECTRIC APPLICAIONS" IEEE TECHNICAL DIGEST:INTERNATIONAL ELECTRON DEVICES MEETING, 11 - 14 December 1994, SAN FRANCISCO, page 117-120 XP002046063 see page 117, column 2, paragraph 2	14

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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